Annika Boyd

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ENGR 271: Digital Logic Design

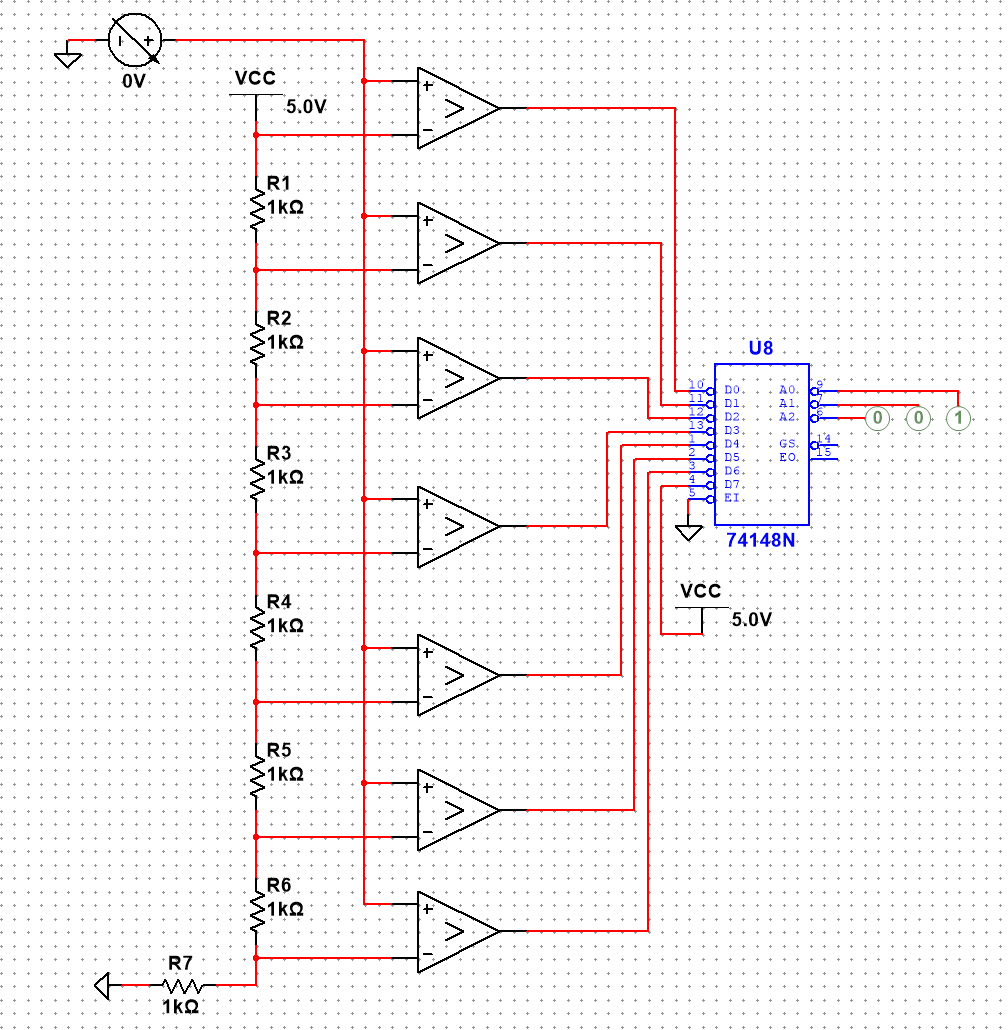
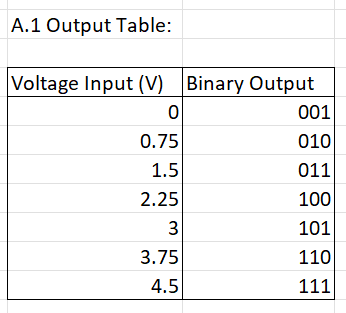
# Lab 12: Analog-to-Digital Conversion (ADC)

## **Introduction**

In this lab, we focused on simulating and understanding two types of analog-to-digital converters. The two types we focused on were the flash ADC and the successive approximation register (SAR) ADC. Learning about these ADCs is important for an electrical engineering student because ADCs play an important role in converting analog to digital signals. This would also be super useful for future projects as an engineer and it provides a solid foundation for dealing with coursework and real-world challenges related to signal processing, system design, and optimization.

## **Part A: Flash ADC**

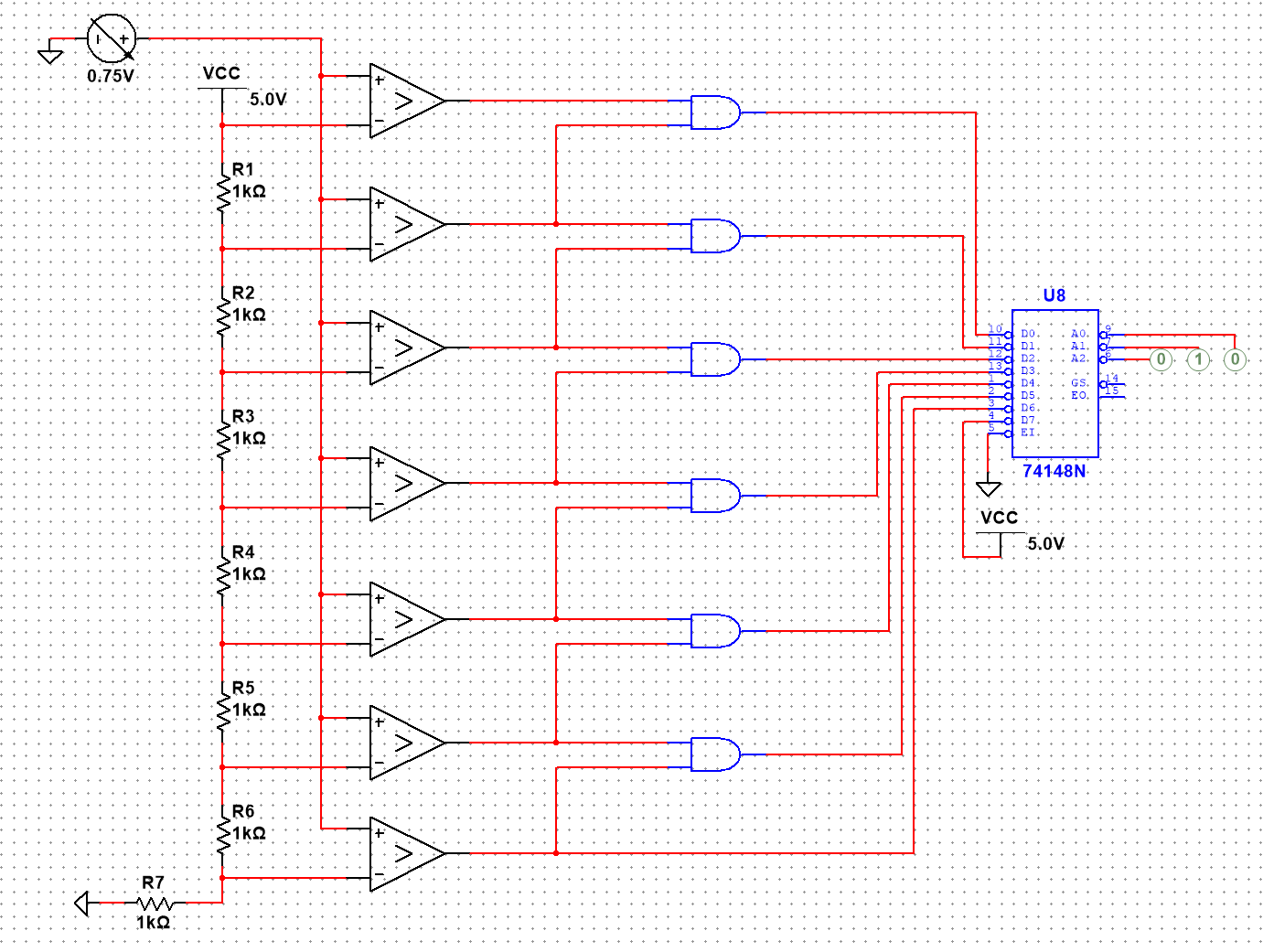
1. In this step, we used Multisim to create the flash ADC given and tested the circuit to ensure that it worked by creating a table.

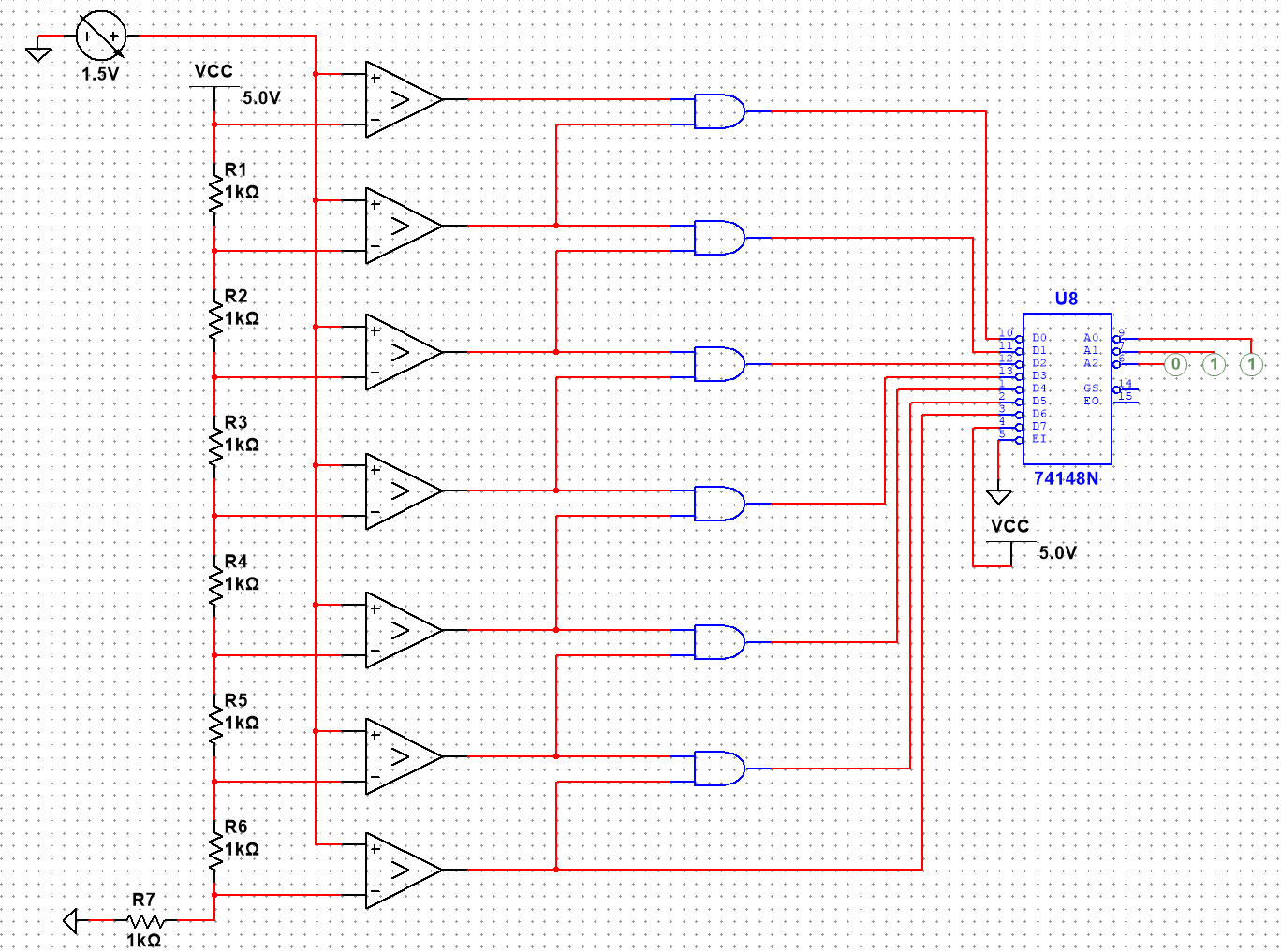


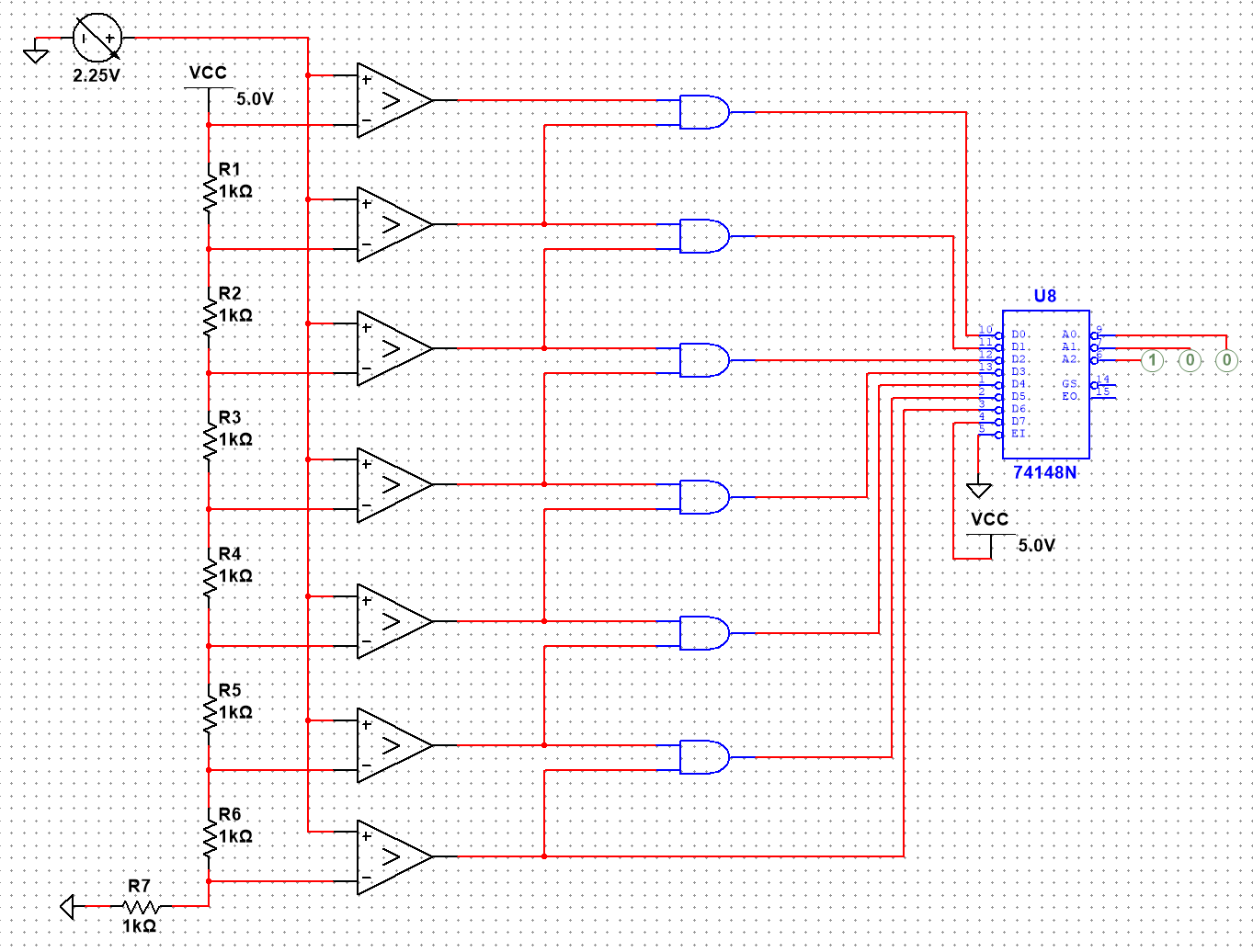
1. In this step, we used datasheets for the components to calculate how fast the flash ADC. From the data sheet, the propagation delay for the LM339 comparator is 15ns and the delay for the 74148 encoder is 10ns. Therefore, the total delay for the flash ADC is the sum of both, being 25 ns. Now, we know that frequency is the inverse of time, so we apply that here and find that the frequency is 40 MHz. Meaning that the speed of the flash ADC is 40MHz.
2. In a flash ADC, the component count grows as the number of bits increases. Specifically, the comparator component increases by a factor of 2n - 1, and the resistor component increases by a factor of 2n, where n represents the number of bits. Consequently, as the number of bits rises, the physical size of the ADC chip must expand exponentially. This growth in size directly impacts the cost of manufacturing the flash ADC.

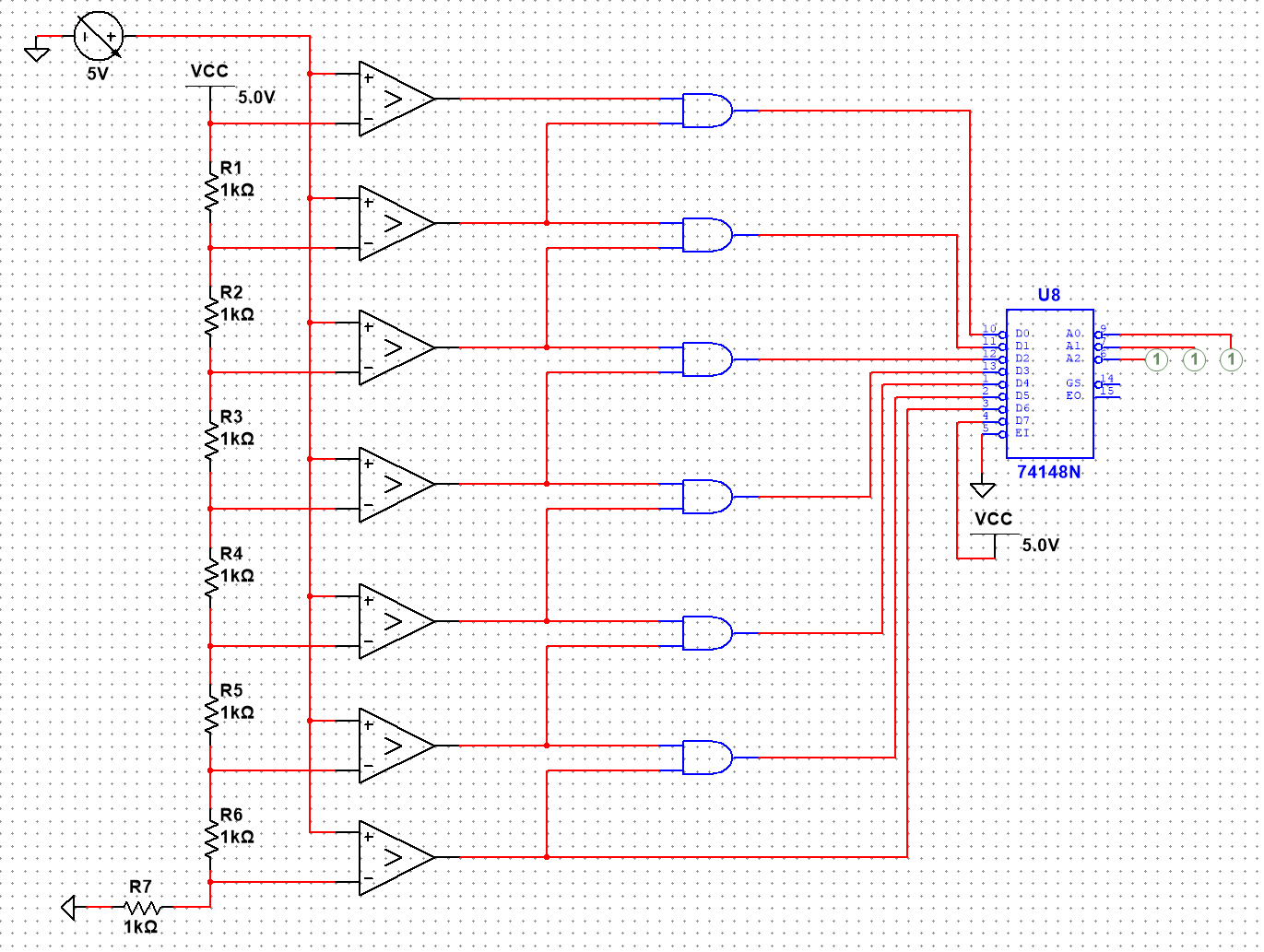
In the flash ADC, the amount of space required on silicon increases two times the number of bits increased by. This is due to the fact that the input voltage is compared to a set of reference voltages generated by a resistor ladder network.

1. In this procedure, we had to design logic for each pair of neighboring comparators that prevents bubble errors (non-thermometer code) from being sent to the priority encoder. To prevent the bubble errors, we realized we had to add AND gates after the comparators, with the exception of the last one. Below are multiple screenshots of the circuit working in multisim.



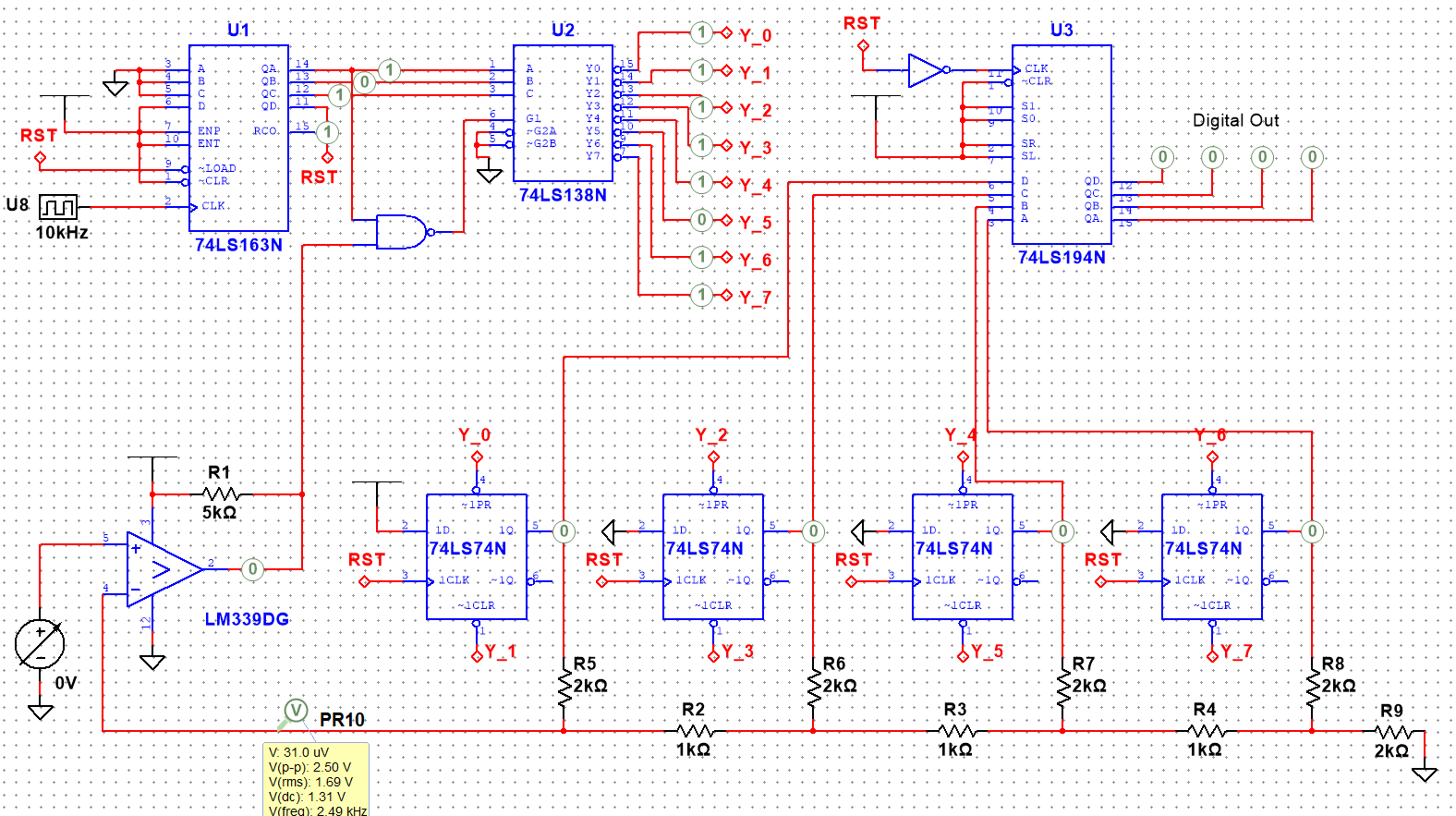


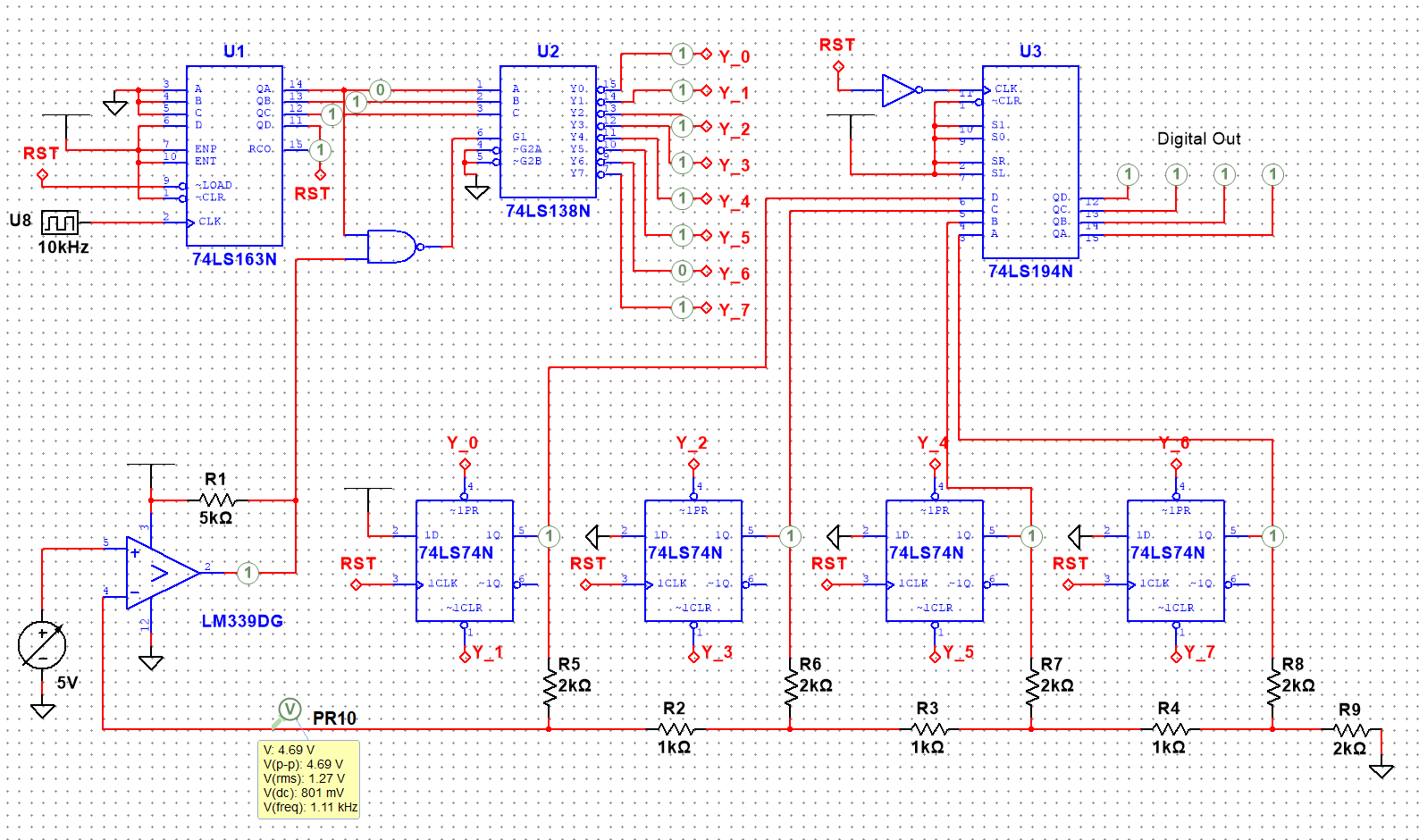


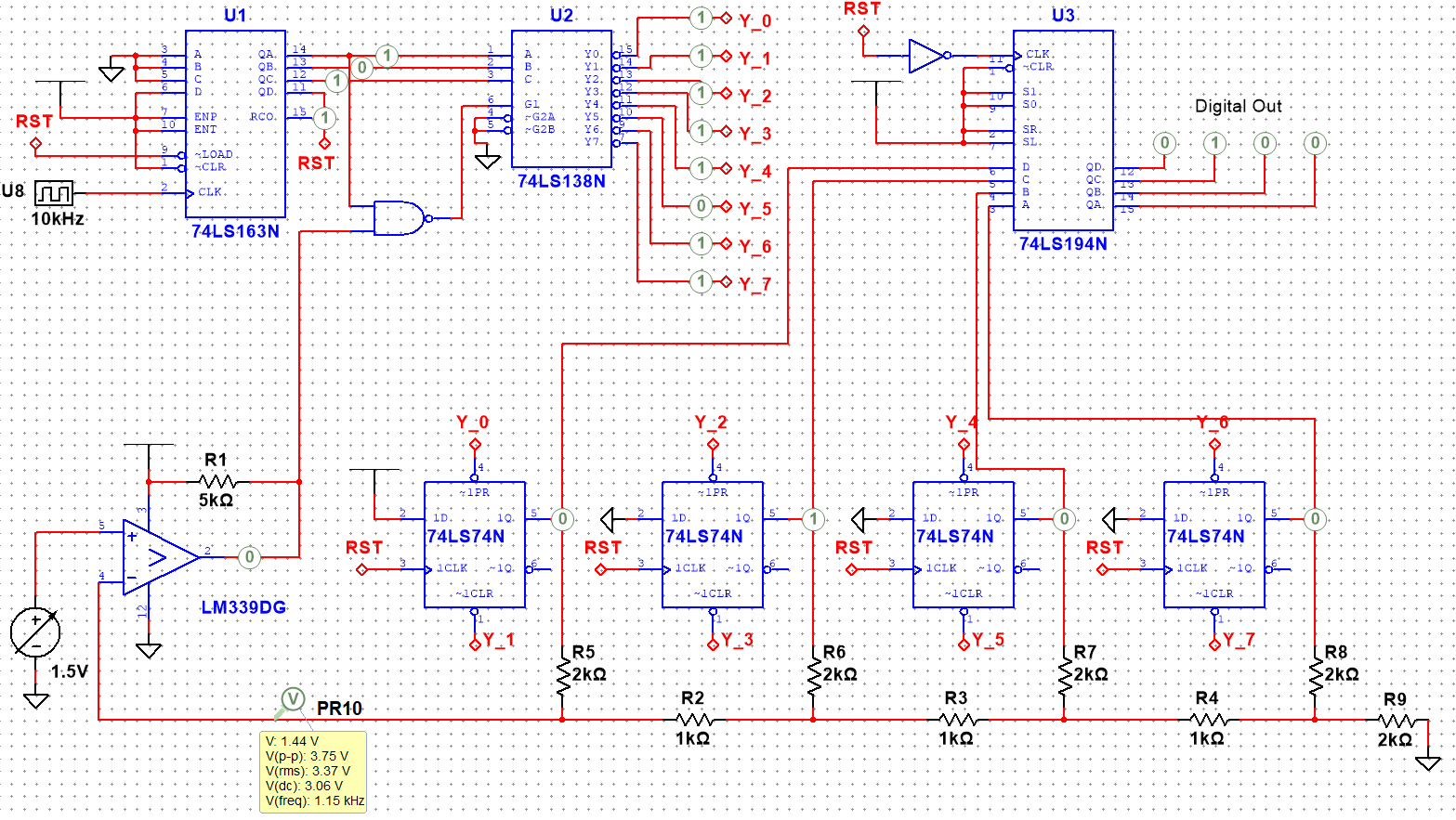


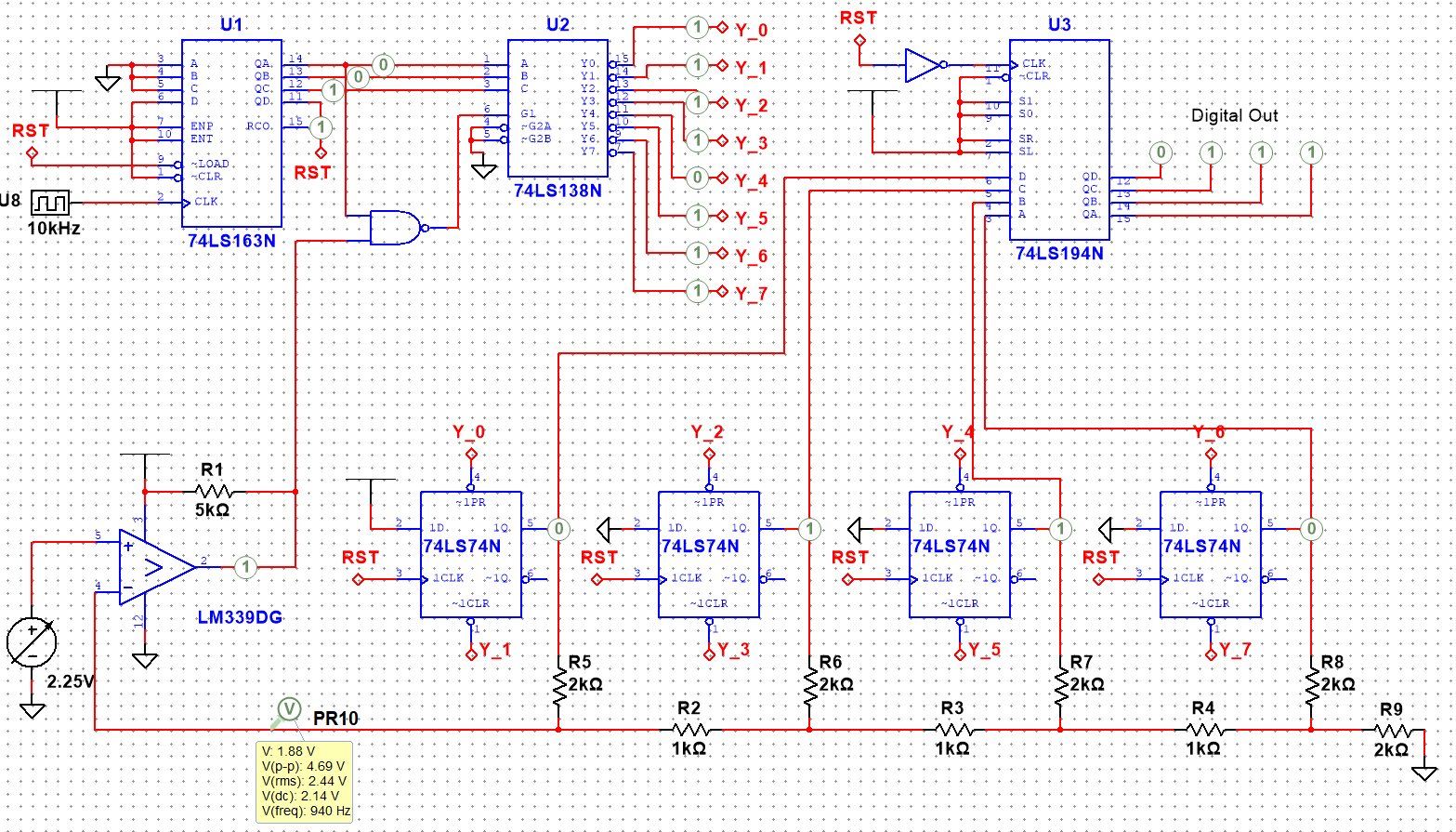
## **Part B: Successive Approximation Register (SAR) ADC**

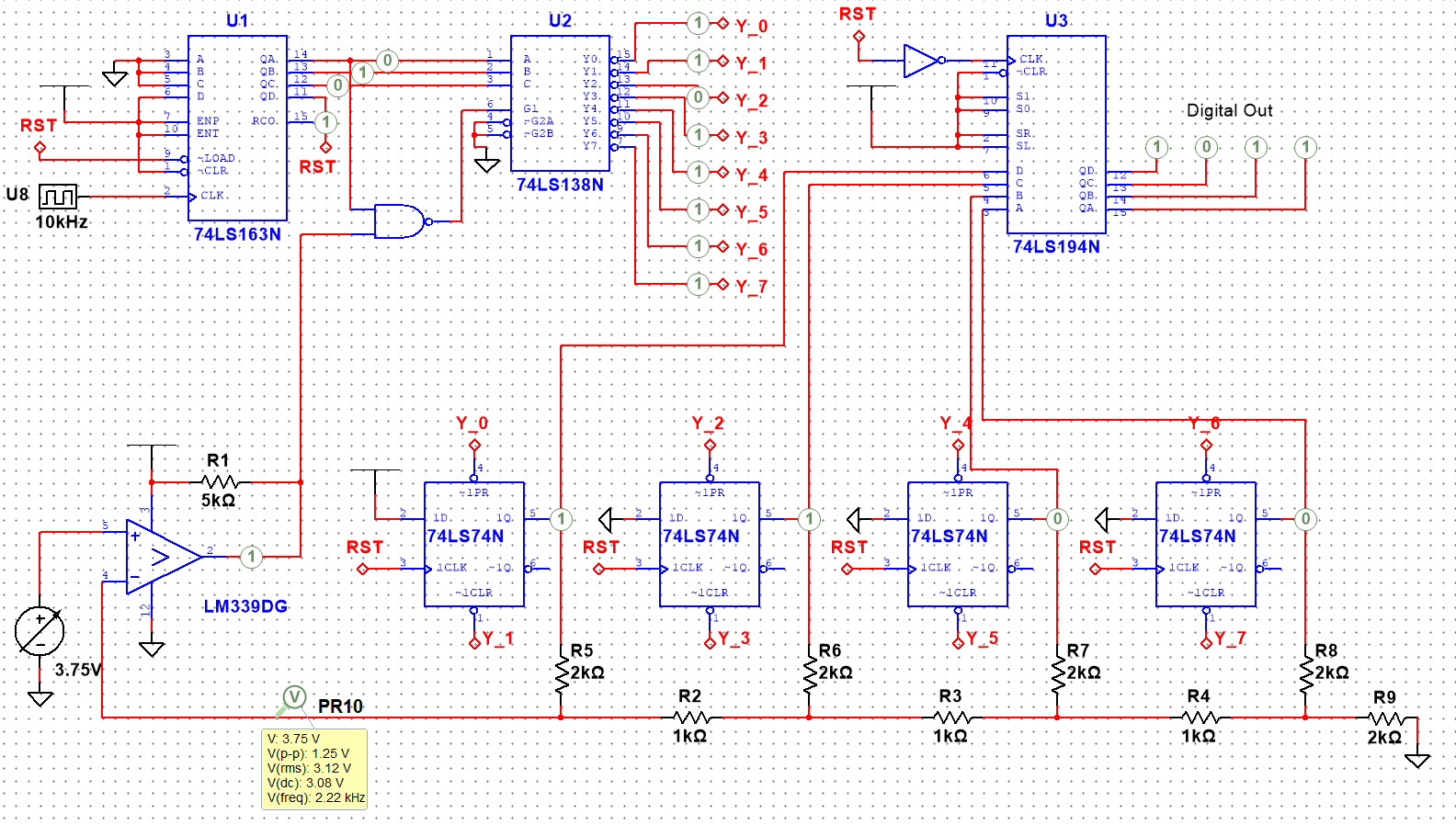
1. In this step, we built the given SAR ADC in multisim and tested the circuit with multiple values. We chose the first two cases to be a 0v case and a 5v case because they are edge cases and that is often where errors appear. Next we chose the same value as the example given to ensure that the circuit was working correctly. The next cases were at 2.25v and 3.75v because we thought it would be a good idea to show more of the cases in the middle, as they weren’t super represented.



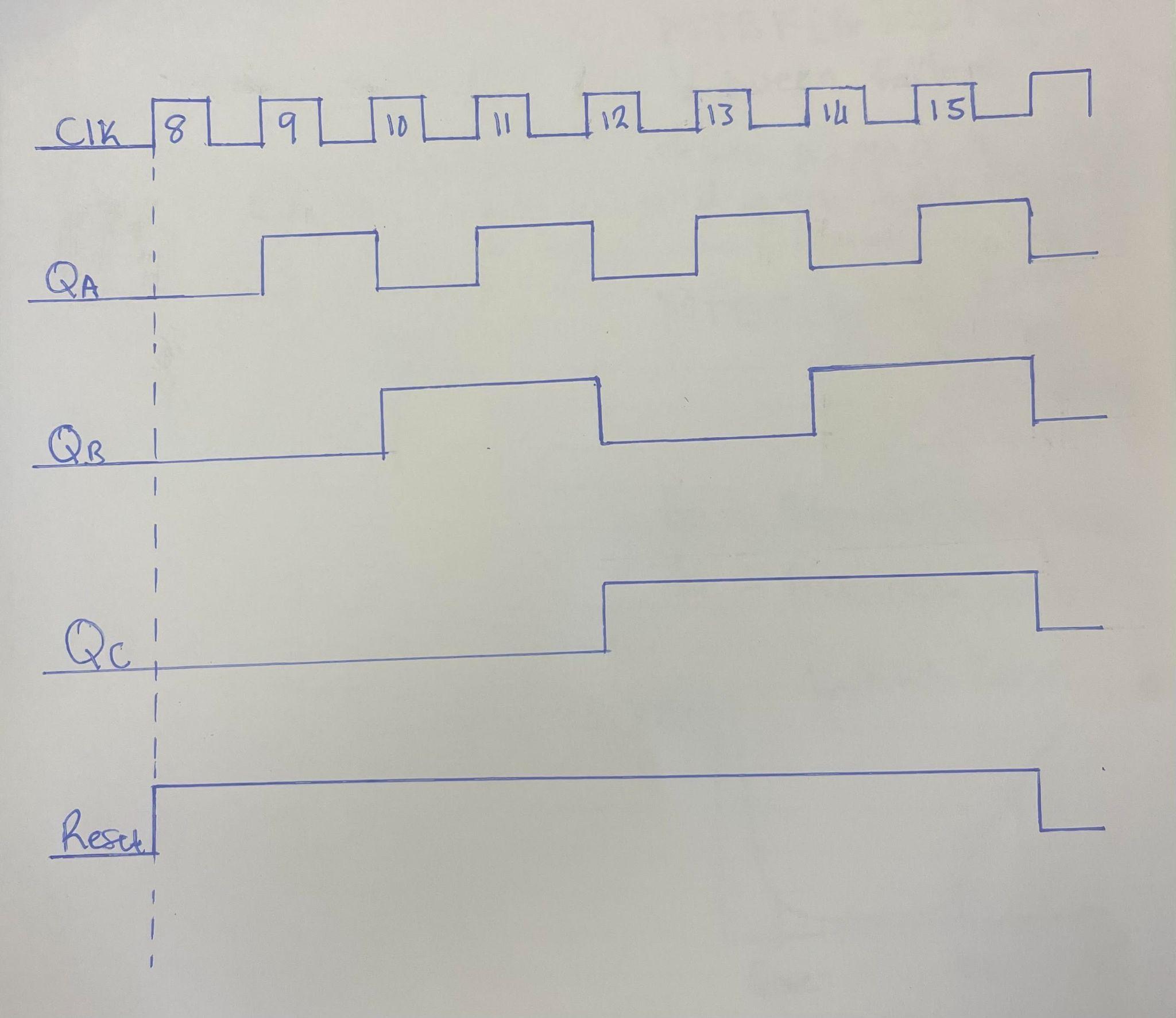








1. In this step, we had to draw a timing diagram for the 74163 IC that showed the CLK, QA, QB, QC and RST signals. This can be seen below, where we also see that the number sequence it is configured to produce is 8-15.



1. The SAR ADC is initialized by configuring the necessary control registers and setting the conversion start. The circuit incorporates a 74163 counter IC to analyze the analog input and generate a digital number at its output. The output from the 74163 is then fed into a 74138 decoder, which produces an 8-bit output based on the 4-bit counter output.

Upon conversion start, the SAR ADC sets the Most Significant Bit (MSB) of the digital output to '1' and sets the remaining bits to '0'. The initial state, Y0, generates an output of 1000 from the D flip flops. Subsequently, Y1 sets the next flip flop, while Y3 potentially clears it. This cycle continues, setting and potentially clearing each bit in the SAR ADC.

The SAR ADC operates in two stages: the setup stage, where each bit is initially set to '1', and the decision stage, which determines whether a bit should be cleared or retained. The decision is made by the comparator, which outputs '1' if the DAC output exceeds the input voltage, and '0' otherwise. Once the conversion restarts, the D flip flops hold the values and transmit them to the 74194, which stores the final value.

Based on the output of the comparator, the SAR ADC determines whether the current approximation is higher or lower than the input voltage. If the comparator output is '1', indicating that the current approximation is higher, the corresponding bit remains set, and the SAR ADC moves to the next lower significant bit.

1. A flash ADC, also known as a parallel ADC or parallel comparator ADC, is an ADC that directly converts analog input voltage into a digital output using voltage comparators. It provides high resolution and good linearity due to the direct mapping of voltage levels to digital outputs, making it suitable for applications that require accurate and linear conversion. However, flash ADCs have limitations such as higher component count, increased power consumption, and higher manufacturing costs compared to SAR ADC architectures. They are also susceptible to mismatches and errors in the comparator network, requiring careful design techniques to mitigate these effects.

On the other hand, a SAR ADC uses a successive approximation algorithm to convert analog input voltage into a digital output. SAR ADCs offer good resolution, moderate conversion speed, and relatively low power consumption compared to the high-speed ADCs like the flash ADC. However, SAR ADCs have slower conversion times since the successive approximation algorithm requires multiple iterations for accurate approximation of the input voltage. SAR ADCs also feature more complex circuitry, including a DAC and a comparator, along with the need for a precise reference voltage source. Nonetheless, SAR ADCs retain a balance between resolution, speed, and power consumption, making them commonly used and handy in many different applications.

## **Conclusion**

In conclusion, this lab provided helpful knowledge about two important types of analog-to-digital converters: the flash ADC and the SAR ADC. The flash ADC offers high resolution and good linearity, but comes with increased component count, power consumption, and manufacturing costs. On the other hand, the SAR ADC has a better balance between resolution, speed, and power consumption, making it a good choice for various applications. If we continued with the themes of this lab, I would say we should either learn about more types of ADCs or look into different areas in the real world where these ADCs are used and for what purposes.